Heavy Ion and Proton-induced Single Event Upset Characteristics of a 3D NAND Flash Memory

Dakai Chen, *IEEE Member*, Edward Wilcox, *IEEE Member*, Raymond Ladbury, *IEEE Member*, Christina Seidleck, Hak Kim, Anthony Phan, and Kenneth LaBel, *IEEE Member*

***Abstract*—We evaluated the effects of heavy ion and proton irradiation for a 3D NAND flash. The 3D NAND showed similar single-event upset (SEU) sensitivity to a planar NAND of identical density in the multiple-cell level (MLC) storage mode. The 3D NAND showed significantly reduced SEU susceptibility in single-level-cell (SLC) storage mode. Additionally, the 3D NAND showed less multiple-bit upset susceptibility than the planar NAND, with fewer number of upset bits per byte and smaller cross sections overall. However, the 3D architecture exhibited angular sensitivities for both base and face angles, reflecting the anisotropic nature of the SEU vulnerability in space. Furthermore, the SEU cross section decreased with increasing fluence for both the 3D NAND and the Micron 16 nm planar NAND, which suggests that typical heavy ion test fluences will underestimate the upset rate during a space mission. These unique characteristics introduce complexity to traditional ground irradiation test procedures.**

***Indexed Terms*— Flash memories, single-event effects, single-event upset, proton radiation effects, heavy ion testing**

I. Introduction

NAND Flash memory has become the dominant mass storage technology in the commercial market, due to its unmatched advantages in density, weight, and cost. However, the rapid development of NAND flash technology is predicated on aggressive scaling of the device physical dimensions. As such, the industry is near the limits of scaling as the tunnel oxide thickness approaches sub-nanometer regime. With the continued shrinking of the tunnel oxide, the intrinsic gate leakage current will significantly degrade power efficiency and prevent adequate charge storage. These challenges may be insurmountable without exploring alternative materials or technologies. One potential replacement is the 3D NAND. In 2013, Samsung commercially released the industry's first vertical 3D NAND technology [1]. The transistors in a 3D NAND are stacked on top of each other in vertical towers. The innovation offers an alternative to further extend the life of the NAND flash.

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The advantages of commercial NAND flash are particularly attractive for satellite applications where space and weight are critical. Many space programs have started to implement state-of-the-art NAND flash in flight applications [2]−[6]. However, the commercial die does not undergo any design or process change to enhance its hardness to the space environment. The flash memory die in satellites are identical to the ones found in consumer electronics (i.e. laptops, mobile phones, and portable drives). Therefore, it is critical to understand the susceptibility of the latest commercial flash memories against the relevant radiation environments and radiation effects, including but not limited to total-ionizing dose (TID), and heavy ion and proton-induced single-event effects (SEE). The radiation effects community has investigated each generation of flash technology [2]−[20]. These investigations included testing for feasibility of specific flight missions [2]–[6], research done by academic institutions [7]−[11], and technology evaluations performed by NASA, ESA, and other aerospace industries [12]−[20]. Notably, the publications on this topic included an early paper in 1997 on a 16 Mbit NOR and a NAND flash [19]. One of the latest publications in 2016 evaluated a 128 Gb planar NAND flash [20]. The devices in the 1997 study were robust against heavy ion-induced single-event upset (SEU). The authors alluded to the introduction of devices with multiple storage levels in the future, which they speculated could introduce further complexity to the radiation response. In fact, more recent studies have shown that SEU susceptibility can be substantial in multiple-level cell (MLC) or triple-level cell (TLC) devices [18], [20]. The results illustrate how the technological progress can impact radiation effects.

The innovation of the 3D NAND can potentially introduce new mechanisms or shift the significance of known effects. Traditionally, SEU in flash has been manageable at a system level with a basic error detection and correction (EDAC) algorithm, given the relatively low SEU rate and the typically extremely low multiple-bit upset (MBU) sensitivity [2], [3] [6], [8], [21]. The 3D structure can potentially alter the SEU characteristics. So, in this paper we focus on the SEU sensitivity for a 3D NAND flash and compare with a planar NAND flash of identical density and similar performance specifications. Both part types are commercially available as standalone memory products. The planar NAND device will likely represent one of the last generations of planar technology, while the Hynix 3D flash is one of the first of the 3D NAND technology.

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II. Experimental

A. Device under test

The Hynix H27QDG822C8R-BCG is a 128 Gb 3D NAND flash available in a plastic encapsulated fine-pitch ball grid array (fBGA) package [22]. Fig. 1 shows a scanning electron microscopy (SEM) image of the device cross section [23]. The array transistors are oxide-nitride-oxide charge-trap flash with gate all around [23]. The architecture features both single-level-cell (SLC) and MLC storage modes. Additionally, the SLC mode includes two program options – firmware (denoted here as SLC-fw) and SLC. We carried out much of the test in SLC-fw mode, but also acquired data in the regular SLC mode for comparison. The planar NAND used for this study is the Micron MT29F128G08CBECBH6, a 128 Gb MLC NAND flash built on a 16 nm CMOS process, available in a plastic encapsulated BGA package.

B. Irradiation facility

Heavy ion irradiation was performed at the Lawrence Berkeley National Laboratory (LBNL) Berkeley Accelerator Space Effects (BASE) Facility with 10 MeV beam and at the Texas A&M University (TAMU) Cyclotron Institute with 15 MeV beam. Table I shows the ion characteristics, including the ion specie, linear energy transfer (LET), range in silicon, and energy. The irradiation was carried out for base angles varying from normal incident to 60° and face angles at 0° and 90°. Four samples were tested with heavy ion irradiation.

The proton testing was carried out at the Massachusetts General Hospital (MGH) Francis Burr Proton Beam Therapy Center. The proton beam was tuned and calibrated for 200 and 100 MeV. We degraded the 100 MeV beam for irradiation at 60 and 22 MeV. The beam was collimated to an approximate square exposure area with a side length of 1.33 cm. The flux varied from approximately 5×10^6 to 1×10^9 p/cm^2/sec. Two samples were tested with proton irradiation.

C. Test method

We designed a custom printed circuit board (PCB) with a microcontroller and BGA footprint as the test fixture. Our test is controlled with an ARM Cortex-M4 microcontroller operating at 120 MHz. The flash chips were mounted on a 4-layer PCB. A power supply was located in the irradiation chamber next to the setup. A USB extension cable was fed from the control room located directly upstairs from the irradiation chamber. The setup at the proton facility was fundamentally similar. The control room was located further away from the irradiation chamber. Therefore, we used an approximately 200 feet long Ethernet cable and Ethernet/USB hubs to interface with the microcontroller. The power supply and one of the USB hubs inside the chamber were shielded with bricks against proton-induced secondary particles. Fig. 2 shows a photograph of the test setup at MGH. We prepared the device-under-test (DUT) for heavy ion irradiation by chemical etching to expose the die surface. The tested data patterns included 00, FF, checkerboard AA and inverse checkerboard 55. The test modes included unpowered, static on (standby), dynamic read, and dynamic erase/program/read/read.

Table I
Heavy-ion species, LET, range, and energy.

Ion	LET (MeV·cm^2/mg)	Range in Si (μm)	Energy (MeV)
B	0.9	306	108
Ne	3.5	175	216
Si	6.1	142	292
Ar	9.7	130	400
Cu	21.2	108	659
Kr	30.9	886	886
Kr (TAMU)	28.8	122	953
Au	85.8	90	1956

III. Heavy ion irradiation

A. SEFI characteristics

Single-event functional interrupt (SEFI) has traditionally been the most worrisome nondestructive radiation effect for modern flash given its disruptive nature and probability of occurrence. While the memory array is relatively robust against SEU, the peripheral circuits are particularly vulnerable to SEE, which can lead to a variety of error modes including but not limited to column/row read errors, block level read errors, and operational hang-ups [7], [19]. These types of errors are commonly categorized as SEFI and can be extremely disruptive to system performance.

Fig. 3 shows the SEFI cross sections for both the Hynix 3D NAND and the Micron planar NAND. The test samples were continuously exercised in either read-only mode or read/erase/write cycle. A power cycle is normally required to recover functionality from a SEFI. For the read-only test mode, the data remained unaffected following a SEFI. The 3D NAND showed a LET threshold of greater than 0.9 MeV·cm^2/mg but less than 3.9 MeV·cm^2/mg. The Micron planar NAND flash showed a LET threshold of less than 9.7 MeV·cm^2/mg. The test results indicate that SEFI remains a concern for 3D NAND flash in space applications.

B. SEU characteristics and pattern dependence

It is important to note that the Micron planar device is built on floating-gate technology, whereas the Hynix 3D device is built on charge-trap technology. Therefore, there are differences in the intrinsic sensitivity to SEU between the two processes. We show the SEU results from the two device types together in order to compare the two architectures and provide a metric for the 3D NAND.

Fig. 4 shows the SEU cross section as a function of effective LET for devices that were irradiated unpowered with checkerboard AA pattern. The Hynix data include the MLC, SLC-fw and regular SLC mode. The SEU sensitivity for either of the SLC modes is significantly lower than that for the MLC mode, particularly near the threshold LET region. The cross section near the LET threshold for MLC mode is approximately an order of magnitude higher than that for SLC-fw mode. The noise margins between the threshold voltage distributions of different program levels are much smaller for the MLC mode, thus leading to the higher SEU

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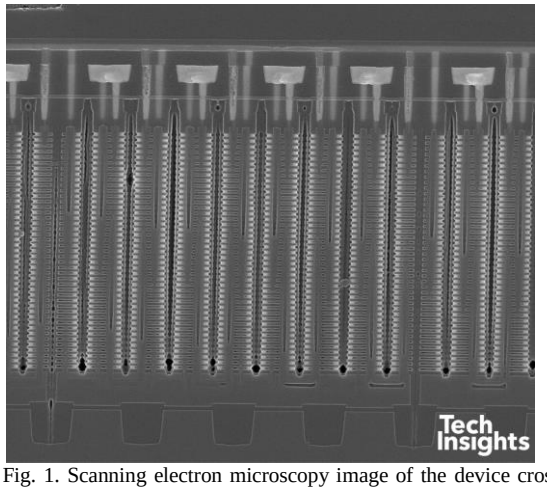

Fig. 1. Scanning electron microscopy image of the device cross section for the Hynix 3D NAND flash [23]. (Published with permission).

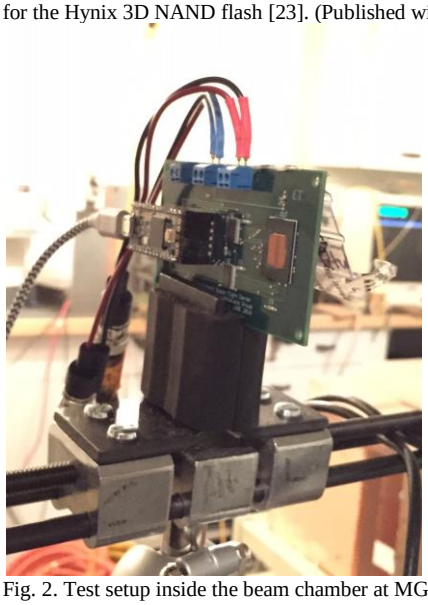

Fig. 2. Test setup inside the beam chamber at MGH.

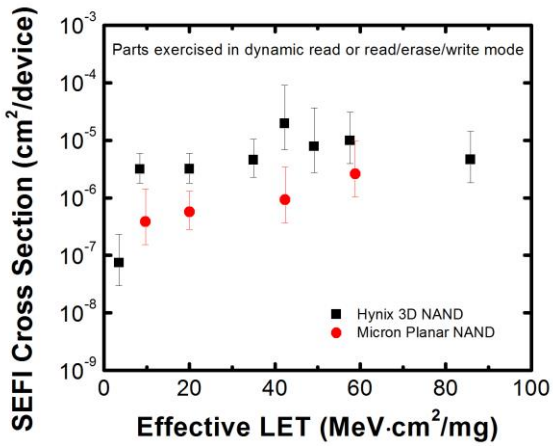

Fig. 3. SEFI cross section vs. effective LET for the Hynix 3D NAND flash and the Micron planar NAND flash.

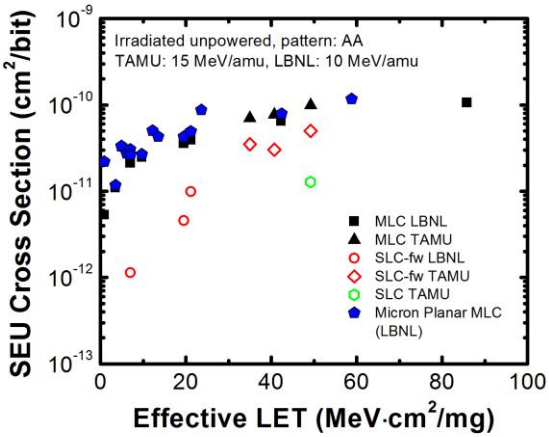

Fig. 4. SEU cross section vs. effective LET for the Hynix 3D NAND flash in MLC, SLC, and SLC-fw storage modes and the Micron planar NAND flash in MLC storage mode.

sensitivity than for the SLC mode. Also, the SLC mode showed even lower sensitivity than the SLC-fw mode in the Hynix 3D NAND. We only obtained a data point for the SLC mode at LET of 49 MeV·cm^2/mg for comparison. The cross sections are fairly similar for the Hynix and Micron for the MLC mode, even though the technology and process nodes are completely different. However, there are differences in the SEU susceptibility between the 3D and planar device with regards to the pattern dependence, angular sensitivity, and MBU characteristics.

Fig. 5 shows the SEU cross section for different data patterns at LET of 9.7 MeV·cm^2/mg. The Hynix 3D NAND showed a range of sensitivities across patterns, while the Micron planar NAND exhibited no pattern dependence. The checkerboard AA and 55 patterns, which represent 10 and 01 binary program levels, showed similar SEU sensitivity in the 3D NAND. This is unlike some earlier generation 50 nm NAND flash devices where the 10 program level showed higher sensitivity than the 01 program level [8]. The magnitude of the threshold voltage shift for a given pattern depends on the position of the threshold voltage relative to the neutral state, which reflects the voltage potential for the stored charges [8].

The results for the 3D NAND suggest that either the 01 and 10 states have similar voltage potentials from the neutral level, or that the threshold voltage distributions are remapped such that those states apparently have similar SEU sensitivities, similar to previous generation 25 nm Micron MLC NAND flash [8]. The lack of sensitivity for the FF pattern suggests that the threshold voltage distribution may be located at or near the neutral level. The 00 pattern showed the highest SEU sensitivity, where most of the upsets were 0 to 1 errors, representing discharge of electrons from the gate. The fact that the cross section of the 00 pattern is more than twice that for either of the checkerboard patterns may be the result of the reduced noise margins for the all 0's state.

C. MBU characteristics and angular sensitivity

A MBU is defined here as a SEU with ≥ 2 upset bits in the same byte. We do not have knowledge of the physical to logical address mapping scheme. However, given the relatively low MBU sensitivity, the memory addresses are most likely interleaved such that the transistors in a vertical

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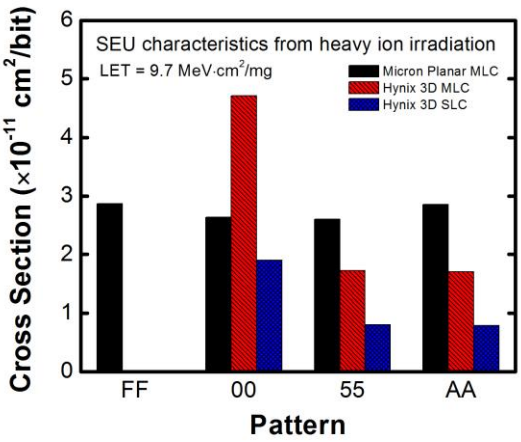

Fig. 5. SEU cross section vs. data pattern for the Hynix 3D NAND flash and the Micron planar NAND flash in different storage modes.

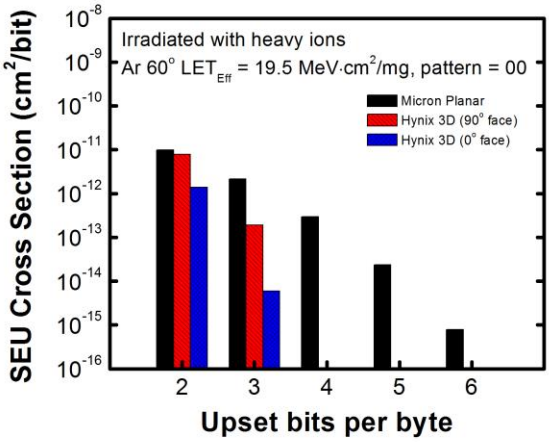

Fig. 6. SEU cross section vs. upset bits per byte for the Hynix 3D NAND and the Micron planar NAND flash in MLC mode, irradiated with Ar at 60° for a LET_{eff} of 19.5 MeV·cm²/mg.

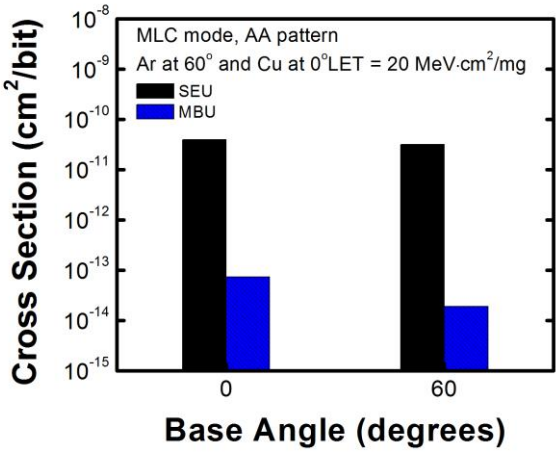

Fig. 7. SEU cross section vs. upset bits per byte for the Hynix 3D NAND flash and the Micron planar NAND flash in MLC mode.

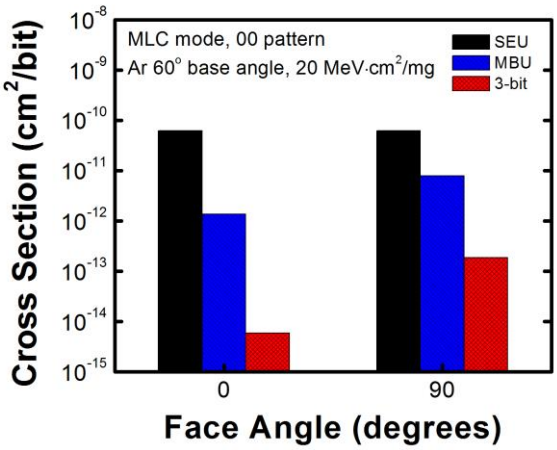

Fig. 8. SEU cross section vs. upset bits per byte for the Hynix 3D NAND flash and the Micron planar NAND flash in MLC mode.

string do not correspond to the same byte for the 3D NAND. Otherwise, normal incident irradiations would cause multiple-cell upsets (MCU) to the strings of vertically stacked transistors, and lead to more large MBUs.

Fig. 6 shows the MBU cross section for the 3D NAND and the planar NAND irradiated with Ar at 60° base angle for an effective LET of 19.5 MeV·cm²/mg. The figure shows that the Hynix 3D NAND is less susceptible to MBU than the Micron planar NAND under the specified test conditions. The Micron planar NAND showed MBUs with up to 6 upset bits per byte compared to 3 upset bits per byte for the 3D NAND. Fig. 6 also shows the MBU cross section for the 3D NAND flash at two face angles.

It is important at this point of the discussion to define the notations for the different axis of rotation. The DUT is mounted directly in front of the source with the die surface perpendicular to the beam line. The east and west directions on the die are defined by the x-axis, and the north and south defined by the y-axis. The depth of the device is defined by the z-axis. We typically rotate the DUT about the y-axis to achieve higher effective LET and examine angular sensitivity. Here, we also examine the effects of rotation about the z-axis. Rotation about the y- and z-axis is denoted by the base and face angle, respectively. Fig. 6 shows that the MBU cross section of the 3D NAND is sensitive to the face angle.

Fig. 7 shows the cross sections for an effective LET of ~20 MeV·cm²/mg at different base angles (Ar at 60° and Cu at normal incidence). The MBU cross section decreased slightly from 0° to 60° base angle. From the fact that the normal incident irradiation showed a much lower MBU cross section than that for SEUs, we can deduce that the memory addresses of the transistors in a vertical string are interleaved to have different logical byte addresses.

Fig. 8 shows the cross sections for irradiation with Ar at 60° base angle and 0° and 90° face angle. The MBU susceptibility of the 3D NAND increased as the face angle increased from 0° to 90°. Also, the magnitude of the increase in cross section from 0° to 90° face angle is more significant for SEUs with higher number of upset bits. The results shown in Fig. 7 and 8 reveal the relation between the ion's path and the device sensitive volume(s). The results suggest that in the case for 0° face angle and 60° base angle, the ion likely traversed through thicker isolation oxides between the transistor strings than for the 90° face angle case.

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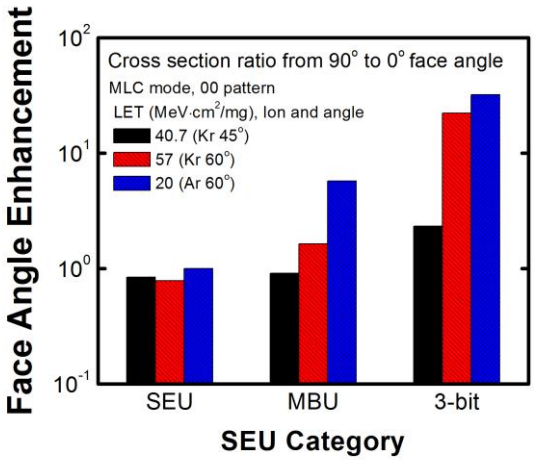

Fig. 9. Normalized cross section of the Hynix 3D NAND from face angle of 90º to 0º for irradiation with Kr at 45º and 60º, Ar at 60º. The cross sections are shown for SEU, MBU, and 3-bit, which include at least 1, 2, and 3 upset bits per byte, respectively.

In addition, we observed that the face angle dependence in the MBU cross section is more significant at higher base angles. Fig. 9 shows the cross section enhancement from 90º to 0º face angle at base angles of 45º and 60º. As shown, the enhancement is greater at 60º than 45º base angle, independent of LET. Irradiation with Ar at 60º for an effective LET of ~20 MeV·cm^2/mg showed greater enhancement than irradiation with Kr at 45º for an effective LET of 40.7 MeV·cm^2/mg. Also, the face angle enhancement increased for increasing number of upset bits per byte, while there is minimal effect to single-bit upsets (SBU) which make up the majority of SEUs. The results in Fig. 9 suggest that the logical addresses of transistors may be mapped across the different transistor strings, such that a byte or word consists of transistors in a row of adjacent strings. Therefore, at a 90º face angle an ion can travel through more vertical strings at higher base angles, and cause more MBUs and larger MBUs.

These results showed that the orientation of the ion's path can significantly impact the MBU sensitivity during heavy ion testing. A thorough evaluation of the MBU sensitivity of the 3D NAND requires testing at multiple base and face angles, representative of the anisotropic nature of heavy ions in the space environment.

D. Fluence dependence

In a previous study, we found that the Micron 128 Gb planar NAND exhibited an inverse fluence dependence for the SEU cross section [20], where the cross section decreased with increasing fluence. We believed that the phenomenon is possible for any high-density device with a variable upset threshold distribution. Here we investigated the fluence dependence for the Hynix 3D NAND flash. Fig. 10 shows the SEU cross section as a function of fluence for the 3D NAND flash at different LETs. The tested fluence ranged from 10^4 to 10^8 ions/cm^2. As shown, the SEU cross section decreased for increasing fluence, similar to the characteristics of the Micron planar NAND flash [20]. The power law curve fits are used to show clarity of data trend.

There are several mechanisms that can arise over time and fluence. One potential effect is annealing over the duration of an irradiation run. To quantify the impact of annealing and/or TID during the irradiation, we carried out irradiations with different durations but the same fluence, and found approximately identical cross sections. We observed the fluence dependence for two irradiation runs with the same duration but different fluence levels. Bagatin et al. have shown that approximately 5% of cell upsets can anneal approximately an hour after irradiation for floating gate NAND flash [24]. The run durations in this study and for typical heavy ion tests are on the order of a few minutes, and the decrease in cross section over fluence can be as high as an order of magnitude. Therefore, annealing is not the primary mechanism under these conditions. Another possible effect is electron injection, which can cause the previously discharged cells to become charged again, leading to a decrease in upset sensitivity with increasing fluence. However, our data showed that the number of 1 to 0 errors are negligible.

We propose a possible mechanism for the fluence dependence observed here. During a heavy ion irradiation run, the ions will strike the die at random locations. The number of struck locations increases in proportion with increasing fluence. While most of the strikes will not result in SEUs, a small portion of ion strikes will produce single cell upsets, and a smaller portion will produce MCUs to surrounding sensitive nodes. For example, a normally incident strike in the 3D NAND can upset several transistors in a vertical string. While those upsets do not result in MBUs, they will manifest as multiple SBUs. Such a vertical structure does not exist in the planar NAND. However, MCUs can more easily occur from transistors adjacent to the struck location, due to the significantly reduced noise margins in the highly-scaled 16 nm node technology. Consequently, an ion strike can have a much larger "impact zone" than the original struck node/location, due to the contribution of MCUs from the surrounding nodes.

As the fluence increases, there is an increasing probability that more than one ion will strike the same cell or strike near the same cell to potentially cause an upset. The presence of an "impact zone" further increases the probability that a cell will be potentially affected by more than one ion strike throughout an irradiation run. So, there will be cases where the impacted cell will already have been discharged from an earlier strike at a lower fluence. A subsequent strike near the same cell will not cause an upset at a higher fluence. In effect, the proportion of the vulnerable cells to ion strikes decreases with increasing fluence. Consequently, the SEUs increase at a slower rate than the increase in the fluence. Thus, the cross section decreases with increasing fluence.

Additional studies may involve measuring the actual threshold voltage levels of the memory cells and/or mapping out the physical locations of the upset cells, which require confidential information from the vendor. We show the following theoretical threshold voltage distributions as visual aid for the discussion. Fig. 11 schematically illustrates the threshold voltage distributions of the struck cells pre- and post-irradiation for a high-density flash. The distribution

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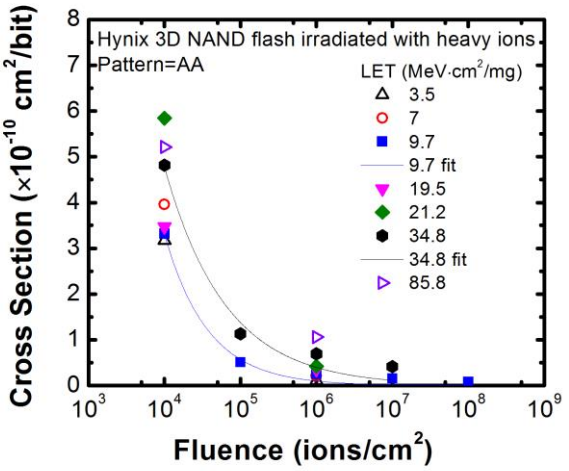

Fig. 10. SEU cross section vs. fluence at different LETs for the Hynix 3D NAND flash. Power law curve fits provided to show trend and clarity.

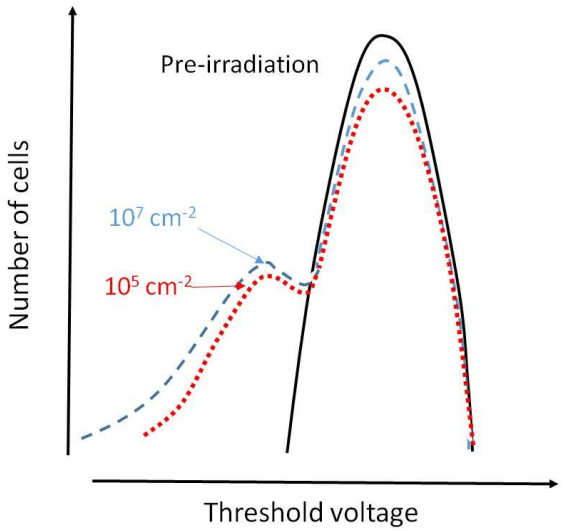

Fig. 11. Schematic diagram showing the threshold voltage distributions for the entire memory pre-irradiation, and the exposed cells population post-irradiation for fluences of 10^5 and 10^7 ions/cm^2. Y-axis is in logarithmic scale and x-axis is in linear scale.

curves after heavy ion irradiation can show a secondary peak, and spreading out in the distribution's left-side tail, based on previous studies [9]. The dotted and dashed curves represent the population of struck cells at a fluence of 10^5 and 10^7 ions/cm^2, respectively.

Due to the relatively poor coverage, the primary peaks of the distributions at the given fluence levels are orders of magnitude lower than the peak in the total population. The primary peak in the distribution at a fluence of 10^7 ions/cm^2 is also shown to be ~2 orders of magnitude higher than that at a fluence of 10^5 ions/cm^2, reflecting the difference in the total number of struck cells between the fluence levels. The effect of the decreasing proportion of vulnerable cells manifests in the narrowing in the shape of the post-irradiation distribution with increasing fluence. Additionally, the difference in the magnitudes of the secondary peaks is shown to be smaller than the difference in the magnitudes of the primary peaks at a fluence of 10^5 and 10^7 ions/cm^2, as a result of the decreasing upset rate.

Previously, we found that the magnitude of the fluence effect increased for decreasing LET for the Micron planar NAND flash [20]. Fig. 12 shows the normalized SEU cross sections for the 3D NAND. The cross section for each LET is normalized to the data at a fluence of 10^4 ions/cm^2. The cross section decreased with increasing fluence more significantly for ions with lower LETs. A possible explanation for the LET dependence is that higher LET ions are able to upset a larger sample of the population with higher threshold voltages. The same population of cells would not be upset by lower LET ions. So, the vulnerable cells make up a larger proportion of the total struck cells at higher LET than at lower LET. Therefore, the magnitude of the fluence dependence decreases for increasing LET.

Furthermore, we found that the fluence effect impacted SBUs more significantly than MBUs. Fig. 13 shows the SBU and MBU normalized cross sections as a function of fluence. The SBU cross section decreased by two orders of magnitude while the MBU cross section remained relatively unchanged, from a fluence of 10^4 to 10^7 ions/cm^2. The Micron planar NAND showed similar characteristics [20]. The probability of a MBU occurring depends on several factors, including the number of vulnerable cells available, the positions of the vulnerable cells in relation to each other, and the location and trajectory of the ion strike. The logical memory addresses are interleaved such that a MCU does not necessarily lead to a MBU, since the cells physically located next to each other do not correspond to the same byte in most cases. So, the positions of vulnerable cells are vital in determining the possibility of a MBU occurring. In addition, the location and trajectory of the ion strike would need to result in sufficient amounts of charge collection at the sensitive nodes of each cell. While the proportion of the number of vulnerable cells to the total number of struck cells will be a function of the fluence, identical to the case for single-bit upsets, the positions of vulnerable cells and the ion strike location and trajectory do not depend on the fluence. Therefore, it is possible that the uncertainties related to the factors that are independence of fluence are more dominant to the total MBU cross section. As a result, we do not observe a fluence effect for MBUs.

The fluence dependence anomaly can potentially impact the accuracy of on-orbit SEU rate calculation using conventional ground test data. A heavy ion test carried out at typical fluence levels will underestimate the on-orbit SEU rate. It may also mean a variable upset rate throughout the mission.

IV. Proton Irradiation

In addition to heavy ion testing, we irradiated two samples of the 3D NAND flash with high energy protons. Protons can cause TID from direct ionization and induce SEE from secondary recoils. We maintained the proton fluence for each irradiation run to an equivalent of ~200 to 600 rad(Si) for each unpowered irradiation run, which was carried out to examine

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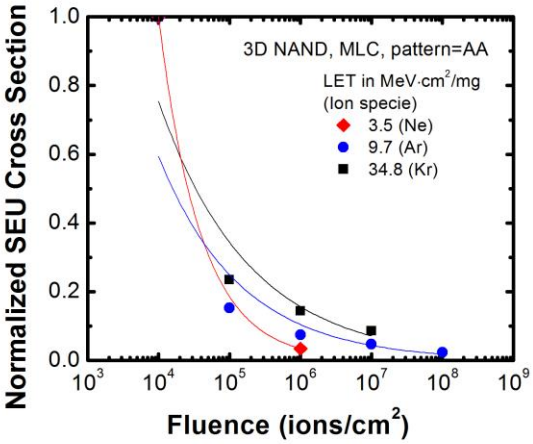

Fig. 12. Normalized SEU cross section vs. fluence for different ions and LETs for the Hynix 3D NAND flash. Power law curve fits provided to show trend and clarity.

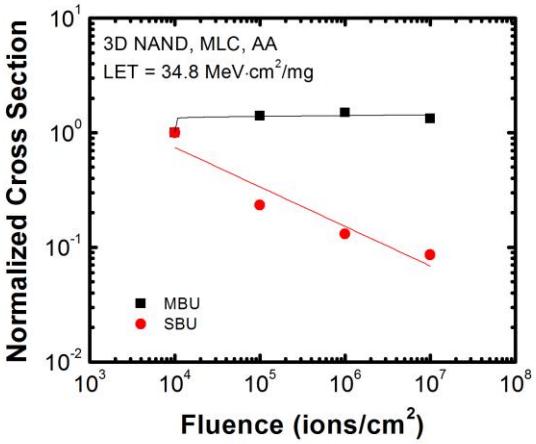

Fig. 13. Normalized SBU and MBU cross section vs. fluence for the 3D Hynix NAND irradiated with Kr for a LET of 34.8 MeV·cm²/mg.

SEU. The part was read, erased, and reprogrammed following each run. The cumulative TID was approximately 25 and 5 krad(Si) for the two samples at the completion of the test. These TID levels are orders of magnitude lower than the level for significant degradation based on Navy Crane's test results [25]. Also, we analyzed two runs under identical beam and bias conditions but at different TID levels (0.5 and 1.8 krad(Si)) and found that the SEU cross sections were similar. Therefore, the effect of TID is secondary to recoil-induced SEUs.

Fig. 14 shows the SEU cross section as a function of proton energy for the MLC and SLC-fw mode with a checkerboard pattern. While the cross section remained relatively flat for the SLC mode, the cross section for the MLC mode increased by ~2 orders of magnitude from 200 to 20 MeV. This characteristic is consistent with the response of a previous generation Micron planar NAND flash [10]. Bagatin et al. showed simulation results of the number of proton secondary by-products in a 41 nm floating-gate cell for proton energies ranging from 35 to 200 MeV. The number of secondary particles with LET below ~7 MeV·cm²/mg increased with

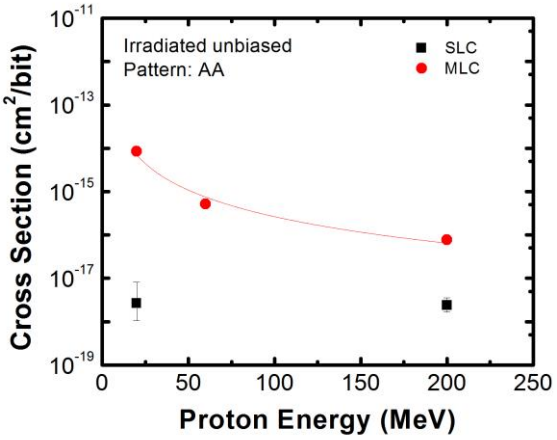

Fig. 14. SEU cross section vs. proton energy for the MLC and SLC-fw mode with checkerboard AA pattern.

decreasing proton energy. The number of secondaries with LET above 7 MeV·cm²/mg increased with increasing proton energy. Our heavy ion test results showed that the SEU LET threshold is less than 0.9 MeV·cm²/mg for the MLC mode and between 3.5 and 7 MeV·cm²/mg for the SLC mode. Therefore, the device in MLC mode is potentially more susceptible to the increase in the number of secondary particles with low LET for decreasing proton energy.

We also observed two SEFIs during the proton test, one each at 60 and 200 MeV, with a cross section of ~5.8×10^{-11} cm² at 60 MeV. The proton-induced SEU rate for the MLC storage mode is still most likely not a concern for the background environments in low earth orbits. However, further studies may be warranted to examine the sensitivity for energies less than 20 MeV.

V. Conclusion

The investigation of the 3D NAND flash showed that SEFI remains a critical concern for space flight applications. Notably, the SLC mode of the 3D NAND offers significant improvement in the SEU tolerance relative to the MLC mode due to the larger technology node of the 3D NAND. The MBU susceptibility of the 3D NAND is improved relative to the planar NAND for the devices here. The 3D NAND exhibited unique angular sensitivities, which necessitate irradiation at various base and face angles to determine a comprehensive representation of the on-orbit performance.

The SEU cross section of the 3D NAND decreased with increasing fluence, similar to the Micron 16 nm planar NAND [20]. Therefore, testing at typical fluence levels may underestimate the on-orbit SEU rate. Although an EDAC can likely manage SBUs for a background environment, high flux situations such as transit through the South Atlantic Anomaly or exposure during a solar particle event may present concerns. A common strategy is to shut down the electronics in those cases. However, the flash memory will be susceptible to SEUs even if it is unpowered. So, it is possible to observe a variable upset rate for the unmitigated or uncorrected errors

that accumulate through the course of a mission. Therefore, it is prudent to consider the effects of the fluence dependence during ground testing.

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